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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WARE, CICELY Q	
ART UNIT	**PAPER NUMBER**
2634	5

DATE MAILED: 03/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/739,860	HOCEVAR ET AL.	
	Examiner	Art Unit	
	Cicely Ware	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-38* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because

   a. Pg. 51, delete line 21

Correction is required. See MPEP § 608.01(b).

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000.

Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 21-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Andoh (US Patent 6,259,749).

(1) With regard to claim 21, Andoh discloses a Viterbi decoder comprising (Fig.2): a state metric update unit (Fig. 2 (12), Fig. 3 (30)) including a state metric memory (Fig. 3 (52)) and a cascaded add/compare/select (ACS) unit (Fig. 3 (41, 42, 43), Fig. 6 (14a, 14b)); and an address generation circuit (Fig. 12 (200, 28, 14a-d)) associated with the ACS unit operative to receive control inputs and generate addresses to control the ACS unit over multiple states of a trellis; wherein the cascaded ACS unit comprises a plurality of serially coupled ACS stages for performing a plurality of ACS operations in conjunction with the state metric memory (Fig. 3 (41,42, 43)).

(2) With regard to claim 22, claim 22 inherits all the limitations of claim 21. Andoh further discloses wherein the address generation circuit is utilized for at least on of read and write operations over multiple stages of the trellis (Fig. 2 (13), Fig. 4(61, 62), Fig. 8a, 8b, Fig. 12 (200, 201a-d)).

(3) With regard to claim 23, claim 23 inherits all the limitations of claim 22. Andoh further discloses the decoder system including controllable counters for address generation (col. 4, lines 49-59, Fig. 2 (20, 15, 12, 13), Fig. 3 (44), Fig. 7 (94)).

(4) With regard to claim 24, claim 24 inherits all the limitations of claim 22. Andoh further discloses the decoder system including a toggle circuit to differentiate nodes of a trellis (col. 3, lines 64-66).

(5) With regard to claim 25, claim 25 inherits all the limitations of claim 22. Andoh further discloses the decoder system including at least one of a phase A operation for reads and a phase B operation for reads (Fig. 4 (61, 62)).

(6) With regard to claim 26, claim 26 inherits all the limitations of claim 22. Andoh further discloses the decoder system including at least one of a phase A operation for writes and a phase B operation for writes (Fig. 4 (61, 62)).

(7) With regard to claim 27, claim 27 inherits all the limitations of claim 21. Andoh further discloses an index generation circuit associated with ACS unit operative to receive control inputs and generate indices to control the ACS unit over multiple stages of a trellis (Fig. 2 (12, 20), Fig. 3 (41, 42, 43, 44)).

(8) With regard to claim 28, claim 28 inherits all the limitations of claim 27. Andoh further discloses wherein the index generation circuit is utilized for at least one of read and write operations over multiple stages of the trellis (Fig. 14 (65)).

(9) With regard to claim 29, claim 29 inherits all the limitations of claim 27. Andoh further discloses the decoder system including controllable counters for index generation (col. 4, lines 49-59, Fig. 2 (20, 15, 12, 13), Fig. 3 (44), Fig. 7 (94)).

(10) With regard to claim 30, claim 30 inherits all the limitations of claim 27. Andoh further discloses the decoder system including a toggle circuit to differentiate nodes of a trellis (col. 3, lines 64-66).

(11) With regard to claim 31, claim 31 inherits all the limitations of claim 27. Andoh further discloses the decoder system including at least one of a phase A operation for reads and a phase B operation for reads (Fig. 4 (61, 62)).

(12) With regard to claim 32, claim 32 inherits all the limitations of claim 27. Andoh further discloses the decoder system including at least one of a phase A operation for writes and a phase B operation for writes (Fig. 4 (61, 62)).

(13) With regard to claim 33, claim 33 inherits all the limitations of claim 27. Andoh further discloses an address and index generation circuit associated with the ACS unit operative to receive control inputs and generate address and indices to control operative to received control inputs and generate addresses and indices to control the ACS unit over multiple stages of a trellis (Fig. 2 (15, 20, 14a,b), Fig. 3 (30, 41, 42, 43), Fig. 12 (200, 14a-d)).

(14) With regard to claim 34, claim 34 inherits all the limitations of claim 33. Andoh further discloses wherein the address and index generation circuit utilized for at least on of read and write operations over multiple stages of the trellis (Fig. 4 (60, 61), Fig. 5a-b, Fig. 12, (200, 201a-d)).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2 and 4-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andoh (US Patent 6,259,749) in view of MUJTABA (US Patent Application 2002/0010895 A1).

(1) With regard to claim 1, Andoh discloses a state metric update including a state metric memory (Fig. 6 (14a, 14b)) and a cascaded Add/Compare/Select (ACS) unit, wherein the cascaded ACS unit comprises a plurality of serially coupled ACS stages for performing a plurality of ACS operations in conjunction with the state metric memory, wherein an ACS stage is operable to identify a plurality of path decisions and communicate the identified path decisions to a next ACS stage coupled thereto (Fig. 3 (30, 41, 42, 43), col. 1, lines 10-22). However Andoh does not disclose a traceback unit for storing a set of accumulated path decisions in a trace back memory associated therewith and performing a traceback on the set of accumulated path decisions, and wherein an ACS data path is widened to receive a Yamamoto quality flag for determining whether an encoded frame contains an error or for use in subsequent quality processing.

However MUJTABA discloses an area-efficient convolutional decoder comprising a traceback unit for storing a set of accumulated path decisions in a trace back memory associated therewith and performing a traceback on the set of accumulated path decisions, and wherein an ACS data path is widened to receive a Yamamoto quality flag for determining whether an encoded frame contains an error or for use in subsequent quality processing (abstract, Pg. 1, col. 2, lines 24-38, Pg. 2, col. 2, lines 13-63, Fig. 5 (16), Pg. 4, 10-38, Fig. 8 (75), Fig. 9).

It is well known in the art that a Yamamoto quality flag is also expressed as a Yamamoto bit.

Therefore it would have been obvious to one of ordinary skill in the art to modify Andoh to incorporate a traceback unit for storing a set of accumulated path decisions in a trace back memory associated therewith and performing a traceback on the set of accumulated path decisions, and wherein an ACS data path is widened to receive a Yamamoto quality flag for determining whether an encoded frame contains an error or for use in subsequent quality processing. The traceback unit is used along the optimal path to extract the corresponding input bits and the Yamamoto bit serves to indicate the robustness of the path elimination process in the ACS engine (MUJTABA Pg. 1, col. 2, lines 31-32, Pg. 4, col. 1, lines 13-15).

(2) With regard to claim 2, claim 2 inherits all the limitations of claim 1. MUJTABA further discloses the decoder system further including a widened state metric memory for processing the Yamamoto quality flag from the widened ACS data path (Pg. 4, col. 1, lines 11-15, col. 2, lines 63-67, Pg. 5, col. 1, lines 1-5, 9-21).

(3) With regard to claim 4, claim 4 inherits all the limitations of claim 1. MUJTABA further discloses wherein at least one of the ACS stages is padded to enable traceback operations on data frames having differing sizes (Pg. 5, col. 1, lines 26-64, col. 2, lines 2-11, 15-41).

(4) With regard to claim 5, claim 4 inherits all the limitations of claim 4. MUJTABA further discloses wherein the at least one ACS stages is padded via a modified ACS operation (Fig. 13, Pg. 2, col. 2, lines 42-48).

(5) With regard to claim 6, claim 6 inherits all the limitations of claim 5. MUJTABA further discloses wherein the modified ACS operation comprises forcing a selection of a

top butterfly node so that traceback may occur from a desired state of zero (Fig. 13, Pg. 1, col. 2, lines 1-7, Pg. 2, col. 2, lines 42-48).

(6) With regard to claim 7, claim 7 inherits all the limitations of claim 5. MUJTABA further discloses wherein the modified ACS operation comprises forcing selection of a top and bottom butterfly node so that traceback may occur form any desired state (Fig. 14).

(7) With regard to claim 8, claim 8 inherits all the limitations of claim 5. MUJTABA further discloses wherein the modified ACS operation comprises forcing a new state metric value equal to a prior state metric value so that state metric values are preserved a the end of the data frame (Pg. 1, col. 1, lines 53-67, col. 2, lines 1-7).

(8) With regard to claim 9, claim 9 inherits all the limitations of claim 5. MUJTABA further discloses wherein the modified ACS operation is communicated to the at least one ACS stages via a code associated with a branch metric for the at least one ACS stage (Pg. 2, col. 1, lines 64-67, col. 2, lines 1-21).

(9) With regard to claim 10, claim 10 inherits all the limitations of claim 5. MUJTABA further discloses wherein the modified ACS operation is communicated to the at least one ACS stages via a signal associated with the decoder system (Fig. 8 (72, 75), Fig. 9 (80)).

7. Claims 11-20 and 35-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over MUJTABA (US Patent Application 2002/0010895 A1) in view of Katsuragawa et al. (US Patent 5,907,586).

(1) With regard to claim 11, MUJTABA discloses an area-efficient convolutional decoder system comprising: a state metric update unit including a state metric memory and a cascaded Add/Compare/Select (ACS) unit, wherein the cascaded ACS unit comprises a plurality of serially coupled ACS stages for performing a plurality of ACS operations in conjunction with the state metric memory (Fig. 7A, 7C, Pg. 2, col. 1, lines 13-21, 40-45), and a Traceback unit for storing a set of accumulated path decisions in a traceback memory associated therewith and performing a traceback on the set of accumulated path decisions (Fig. 9 (92)) wherein the path decisions associated with the ACS stage and the next ACS stage are accumulated as a set during the ACS operations before being written to the traceback memory, thereby minimizing accesses to the traceback memory (Pg. 2, col. 2, lines 42-63). However MUJTABA does not discloses wherein an ACS stage is operable to identify a plurality of path differences and communicated the identified path differences to a next ACS stage coupled thereto; and wherein the path differences associated with the ACS stage and the next ACS stage provide a reliability estimation of the correctness of the path decisions.

However Katsuragawa et al. discloses a channel condition estimating method wherein an ACS stage is operable to identify a plurality of path differences and communicated the identified path differences to a next ACS stage coupled thereto; and wherein the path differences associated with the ACS stage and the next ACS stage

provide a reliability estimation of the correctness of the path decisions (col. 2, lines 59-61, col. 4, lines 21-24, col. 15, lines 65-67, col. 16, lines 1-37, 64-67, col. 17, lines 1-5).

Therefore it would have been obvious to one of ordinary skill in the art to modify MUJTABA to incorporate wherein an ACS stage is operable to identify a plurality of path differences and communicated the identified path differences to a next ACS stage coupled thereto; and wherein the path differences associated with the ACS stage and the next ACS stage provide a reliability estimation of the correctness of the path decisions in order to reduce the error frequency of signal decision with more accurate indexes for channel condition estimation (Katsuragawa et al., col. 3, lines 54-59).

(2) With regard to claim 12, claim 12 inherits all the limitations of claim 11. Katsuragawa et al. further discloses wherein the ACS stage is operable to identify the path decisions by utilizing the path differences (col. 16, lines 1-39, col. 17, lines 1-5).

(3) With regard to claim 13, claim 13 inherits all the limitations of claim 11. Katsuragawa et al. further discloses wherein the identified path differences are accumulated as a set by forwarding the identified path differences from the ACS stage to the next ACS stage during ACS operations (col. 15, lines 65-67, col. 16, lines 1-37).

(4) With regard to claim 14, claim 14 inherits all the limitations of claim 13. Katsuragawa et al. further discloses wherein the identified path differences are accumulated as a set by widening an ACS data path to receive the identified path differences form the ACS stage and forwarding the identified path differences to the next ACS stage (Fig. 1, Fig. 5A (110, 120), col. 2, lines 9-18, col. 15, line 67, col. 16, lines 1-3).

(5) With regard to claim 15, claim 15 inherits all the limitations of claim 14. Katsuragawa et al. further discloses wherein the accumulated set of path differences are routed form the ACS stage into a path selection circuit within the next ACS stage (col. 15, lines 65-67, col. 16, lines 1-37).

(6) With regard to claim 16, claim 16 inherits all the limitations of claim 15. Katsuragawa et al. further discloses wherein the path selection circuit is operable to accumulate the identified path differences by combining the identified path differences from the ACS stage with identified path differences from the next ACS stage (Fig. 7, col. 15, lines 65-67, col. 16, lines 1-37).

(7) With regard to claim 17, claim 17 inherits all the limitations of claim 16. Katsuragawa et al. further discloses wherein the combined identified path differences are maintained in the widened ACS data path (col. 2, lines 9-18, col. 15, line 67, col. 16, lines 1-3).

(8) With regard to claim 18, claim 18 inherits all the limitations of claim 15. Katsuragawa et al. further discloses wherein the path selection circuit further comprises at least on multiplexer for selecting and routing identified path differences to the next ACS stage, and at least on appending circuit for combining path differences from the ACS stage with the identified path differences from the next ACS stage (col. 17, lines 12-65).

(9) With regard to claim 19, claim 19 inherits all the limitations of claim 11. Katsuragawa et al. further discloses wherein the path differences and path decisions are stored in memory, wherein an address portion associated with the path difference

relates to an address portion associated with the path decisions, wherein the associated address portion of the path differences are utilized to retrieve the path decisions stored in memory (Fig. 7 (460, 490, 480), Fig. 11, col. 17, lines 1-11, col. 20, lines 28-39, 65-67, col. 21, lines 1-10).

(10) With regard to claim 20, claim 20 inherits all the limitations of claim 11. Katsuragawa et al. further discloses wherein the path differences and path decisions are stored in memory, wherein an address portion associated with the path difference relates to an address portion associated with the path decisions, wherein the associated address portion of the path decision are utilized to retrieve the path differences stored in memory (Fig. 7 (460, 490, 480), Fig. 11, col. 17, lines 1-11, col. 20, lines 28-39, 65-67, col. 21, lines 1-10).

(11) With regard to claim 35, claim 35 inherits all the limitations of claim 11. Katsuragawa et al. further discloses a Viterbi decoder system identifying a plurality of path decisions and path differences; communicating the identified path decisions and identified path differences to a next ACS stage coupled thereto (col. 6, lines 45-67, col. 7, lines 1-6, col. 15, lines 65-67, col. 16, lines 1-38).

(12) With regard to claim 36, claim 36 inherits all the limitations of claims 35 and 13.

(13) With regard to claim 37, claim 37 inherits all the limitations of claims 36 and 14.

(14) With regard to claim 38, claim 38 inherits all the limitations of claim 37. MUJTABA further discloses in (Fig. 9) the step of including a Yamamoto quality flag in

the widened ACS for determining whether an encoded frame contains an error or for use in subsequent quality processing (Pg. 4, 10-38).

Allowable Subject Matter

8. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made record of and not relied upon is considered pertinent to applicant's disclosure:

a. Mujtaba US Patent 6,477,680 discloses a convolutional decoder.

b. Zehavi US Patent 5,469,452 discloses a Viterbi decoder bit efficient chainback memory.

c. Collins et al. US Patent 5,068,859 discloses a method of formulating and packaging decision-making elements.

d. Cesari et al. US Patent 5912908 discloses a method of efficient branch metric computation for a Viterbi convolutional decoder.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cicely Ware whose telephone number is 703-305-8326. The examiner can normally be reached on Monday – Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Cicely Ware

cqw
March 2, 2004

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